

Area/Energy-Efficient Gammatone Filters Based on Stochastic Computation

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Abstract—This paper introduces area/energy-efficient gammatone filters based on stochastic computation. The gammatone filter well expresses the performance of human auditory peripheral mechanism and has a potential of improving advanced speech communications systems, especially hearing assisting devices and noise robust speech-recognition systems. Using stochastic computation, a power-and-area hungry multiplier used in a digital filter is replaced by a simple logic gate, leading to area-efficient hardware. However, a straightforward implementation of the stochastic gammatone filter suffers from significantly low accuracy in computation, which results in a low dynamic range (a ratio of the maximum to minimum magnitude) due to a small value of a filter gain. To improve the computation accuracy, gain-balancing techniques are presented that represent the original gain as the product of multiple larger gains introduced at the second-order sections. In addition, dynamic scaling techniques are proposed that scales up small values only on stochastic domain in order to reduce the number of stochastic bits required while maintaining the computation accuracy. For performance comparisons, the proposed stochastic gammatone filters are designed and evaluated on taiwan semiconductor manufacturing company (TSMC) 65-nm CMOS technology. As a result, the proposed filter achieves an area reduction of 90.7% and an energy reduction of 91.8% in comparison with a fixed-point gammatone filter at the same sampling frequency and a comparable dynamic range.

Index Terms—Auditory filter, digital circuit implementation, gammatone filter, infinite impulse response (IIR) filter, static power dissipation, stochastic logic.

I. INTRODUCTION

BRAINWARE (brain-inspired) computing-based LSI (BLSI) has been recently studied that achieves a significant cognition capability compared with a traditional computation-based approach [1], [2]. The brainware systems can be integrated in Internet-of-things (IoT) devices, if BLSIs

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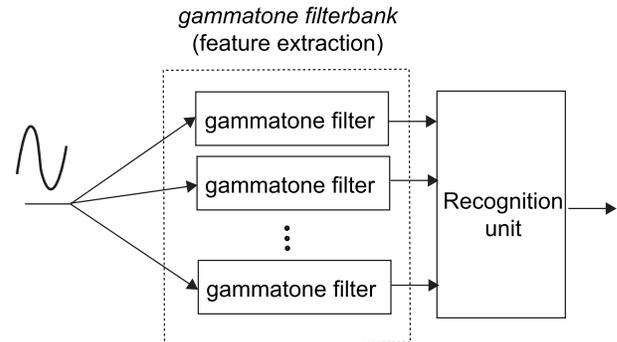


Fig. 1. Brainware speech-recognition system based on the gammatone filterbank.

are designed at ultralow area and energy dissipation. For brainware auditory signal processing, a gammatone filter that has a similar response to the impulse responses of basilar membrane [3], [4] is a promising technique for advanced speech communications systems, such as cochlear implants [5]–[8] and noise robust speech recognitions [9], [10], as shown in Fig. 1.

However, the gammatone filter requires high computational power as the function of the gammatone filter is complicated. Several VLSI implementations have been studied using analog [5]–[7], [10] or digital circuits [8]. In analog implementations, the complicated function of the gammatone filter is efficiently designed, leading to low-power and low-area hardware, while they suffer from process variations, especially in advanced CMOS processes. In digital implementations, the gammatone filter is designed using a high-order infinite impulse response (IIR) filter that contains adders, multipliers, and delay elements. As the multipliers dominate the hardware resource of the IIR filters, a large number of multipliers required cause large power dissipation and large area.

In this paper, we introduce an area/energy-efficient gammatone filter based on *stochastic computation*. In general, stochastic computation [11], [12] designed using digital circuits represents data as streams of random bits, while a power-and-area hungry multiplier used in a digital IIR filter is replaced by a simple logic gate, leading to area-efficient hardware.

The area efficiency is exploited for the hardware implementation of a stochastic gammatone filter.

First, a stochastic gammatone filter is designed using a straightforward implementation technique and is then analyzed in terms of a dynamic range.

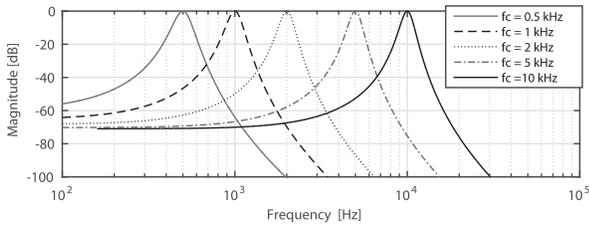


Fig. 2. Frequency responses of five gammatone filters, where f_c are 0.5, 1, 2, 5, and 10 kHz.

Note that the dynamic range is used as a ratio of the maximum to minimum magnitude throughout this paper. Based on the analysis, the straightforward implementation suffers from significantly low computation accuracy due to a small value of a filter gain, which results in a low dynamic range. To improve the computation accuracy, gain-balancing techniques are presented. In the gain-balancing techniques, the original gain is represented by the product of multiple larger gains introduced at the second-order sections, avoiding the small value of the filter gain represented using stochastic bit streams. In addition, dynamic scaling techniques are proposed in order to avoid using small values of signals represented by stochastic bit streams. These techniques dynamically scale up small values only on stochastic domain, reducing the number of stochastic bits required while maintaining the computation accuracy. For performance comparisons, the proposed stochastic gammatone filters are designed using Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS technology and are compared with fixed-point and analog implementations. To the best of our knowledge, this is the first hardware algorithm and architecture of a gammatone filter based on stochastic computation.

The short version of this paper [13] presented limited results at algorithm level, but the extended version presented in this paper includes the following:

- 1) dynamic scaling techniques to reduce the number of stochastic bits;
- 2) design and synthesis of the proposed stochastic gammatone filters using Verilog-HDL and TSMC 65-nm CMOS technology;
- 3) performance comparisons with fixed-point implementations designed as baseline and analog implementations previously published.

The rest of this paper is organized as follows. Section II reviews the gammatone filter and designs it using cascaded second-order sections. Section III describes the stochastic gammatone filters based on the gain-balancing techniques. Section IV shows the circuit implementation of the stochastic gammatone filters. Section V presents the dynamic scaling techniques. Section VI evaluates the magnitude responses of the stochastic gammatone filters and compares the performance with fixed-point and analog implementations. Section VII concludes this paper.

II. REVIEW OF GAMMATONE FILTERS

A. Transformation of Gammatone Filters to Digital Domain

A gammatone filter is represented by an impulse response that is the product of a gamma distribution and a sinusoidal

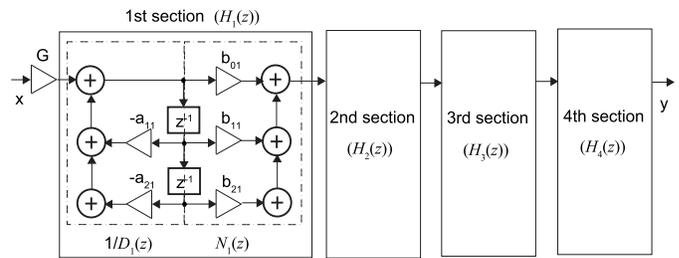


Fig. 3. Block diagram of four cascaded second-order sections for gammatone filters.

tone as follows:

$$g(t) = at^{n-1}e^{-2\pi b\text{ERB}(f_c)t} \cos(2\pi f_c t + \phi) \quad (t > 0) \quad (1)$$

where a is a constant, n is the order of the filter, b is the bandwidth of the filter, f_c (Hz) is the center frequency of the filter, and ϕ is the starting phase. The equation can represent the human auditory filter when n is 4 and b is 1.019 times equivalent rectangular bandwidth (ERB) [3]. The ERB can be approximated [4] as follows:

$$\text{ERB}(f_c) = 24.7(4.37f_c/1000 + 1). \quad (2)$$

In this paper, a is set to 1 and ϕ is set to 0 as in [7]. The frequency responses of the gammatone filters are shown in Fig. 2, where f_c are 0.5, 1, 2, 5, and 10 kHz.

The gammatone impulse response is converted to that in the frequency domain using the Laplace transform, which is then converted to a digital IIR filter using the bilinear transform with an f_c of 5 kHz and a sampling frequency, f_s , of 20 kHz used in this paper. The transfer function in digital domain, $H(z)$, is described using an eighth-order digital IIR filter as follows:

$$H(z) = \frac{b_0 + b_1z^{-1} + \dots + b_8z^{-8}}{1 + a_1z^{-1} + \dots + a_8z^{-8}} \quad (3)$$

where b_n ($0 \leq n \leq 8$) and a_m ($1 \leq m \leq 8$) are coefficients.

B. Implementation Using Cascaded Second-Order Sections

To reduce the computation complexity, the eighth-order IIR filter for the gammatone response in (3) is factorized to form four second-order sections as follows:

$$H(z) = G \prod_{k=1}^4 \frac{b_{0k} + b_{1k}z^{-1} + b_{2k}z^{-2}}{1 + a_{1k}z^{-1} + a_{2k}z^{-2}} \quad (4)$$

$$= G \prod_{k=1}^4 H_k(z) = G \prod_{k=1}^4 \frac{N_k(z)}{D_k(z)} \quad (5)$$

where G is a gain, and the transfer function of the feedforward block is defined as $N_k(z)$ and that of the feedback block is defined as $1/D_k(z)$. The four second-order sections are described as shown in Fig. 3, where each section is designed using a second-order IIR filter.

Fig. 4 shows magnitudes of frequency responses in the four cascaded second-order IIR filter for a gammatone response at an f_c of 5 kHz and an f_s of 20 kHz. At each section, the maximum magnitude of the transfer function, $\max|H_k(e^{j\omega})|$, is

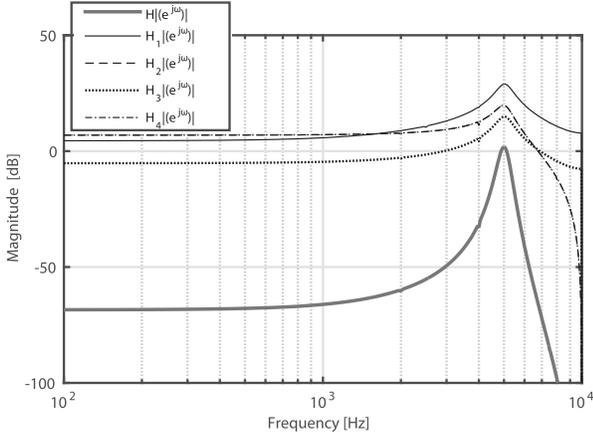


Fig. 4. Magnitudes of frequency responses in the four cascaded second-order IIR filter for a gammatone response at an f_c of 5 kHz and an f_s of 20 kHz.

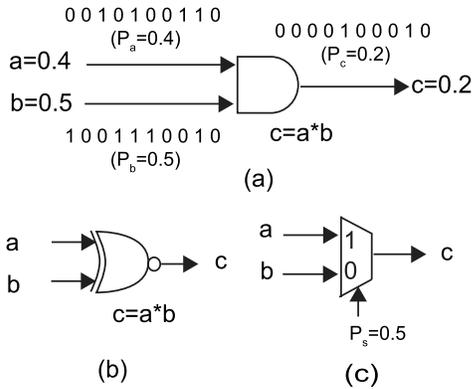


Fig. 5. Stochastic computation blocks. (a) Multiplier in unipolar coding. (b) Multiplier in bipolar coding. (c) Scaled adder.

larger than 1. In contrast, the maximum magnitude of the transfer function, $\max|H(e^{j\omega})|$, is 1 (0 dB) as G is 6.795×10^{-5} . In the next section, a gammatone filter based on stochastic computation is designed using the four cascaded IIR filters.

III. STOCHASTIC IMPLEMENTATION OF GAMMATONE FILTERS

A. Stochastic Computation

Stochastic computation has been recently exploited for several applications, such as low-density parity-code decoding [14], [15], turbo decoding [16], MIMO decoders [17], image processing [18]–[20], and digital filters [21]–[23]. In stochastic computation, information is carried by the frequency of ones in a sequence in one of two formats: *unipolar* and *bipolar* coding. Note the probability of observing a ‘1’ to be $P_a = \Pr(a(t) = 1)$ for a sequence of bits $a(t)$. A value a is $a = P_a$, ($0 \leq a \leq 1$) in *unipolar* coding and is $a = (2 \cdot P_a - 1)$, ($-1 \leq a \leq 1$) in *bipolar* coding. A value can also be represented by a fraction of the time that the signal is high (logic ‘1’) in polysynchronous stochastic circuits [24].

A multiplier is simply designed using a simple logic gate [12], such as a two-input AND gate in unipolar coding or a two-input XNOR gate in bipolar coding shown in Fig. 5(a) and (b). The output probability, P_c , is $P_a \cdot P_b$

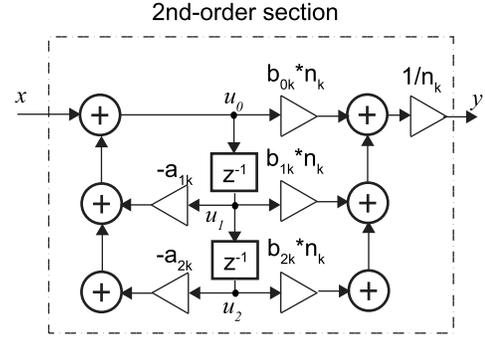


Fig. 6. Second-order section using normalized coefficients for stochastic computation.

in unipolar coding. In the example shown in Fig. 5(a), input values are represented using 10 bits and are multiplied with ten clock cycles. In bipolar coding as shown in Fig. 5(b), the XNOR gate produces $(1 - P_a) \cdot (1 - P_b) + P_a \cdot P_b = ((a + 1) \cdot (b + 1) + (1 - a) \cdot (1 - b)) / 4 = (a \cdot b + 1) / 2 = (c + 1) / 2 = P_c$. Fig. 5(c) shows a block diagram of a two-input scaled addition designed using a two-input multiplexer, unlike a binary full adder. The output probability, P_c , is $P_s \cdot (P_a + P_b)$, where P_s is a probability of a selector input to the multiplexor.

B. Normalized Coefficients

The gammatone filter is designed using the IIR filter with cascaded form consisting of four second-order sections shown in Fig. 3, where the magnitude responses are summarized in Fig. 4. In the filter, the absolute values of several coefficients, b_{0k} , b_{1k} , and b_{2k} , are larger than ‘1.’ For example, b_{21} is -4.7077 . These coefficients need to be normalized as stochastic computation can represent a value of -1 to 1 [23]. The normalizing factor, n_k , is defined as follows:

$$n_k = \frac{1}{m_k} \quad (6)$$

$$m_k \geq \max(|b_{0k}|, |b_{1k}|, |b_{2k}|) \quad (7)$$

where $m_k = \{2^l \mid l = 0, 1, \dots\}$.

The normalized second-order section is illustrated in Fig. 6. The output value, y , is defined as follows:

$$y = ((b_{0k} \cdot n_k) \cdot w_0 + (b_{1k} \cdot n_k) \cdot u_1 + (b_{2k} \cdot n_k) \cdot u_2) / n_k \quad (8)$$

where u_0 , u_1 , and u_2 are the internal values. u_0 is defined as follows:

$$u_0 = x - a_{1k} \cdot u_1 - a_{2k} \cdot u_2. \quad (9)$$

Using (6), the transfer function at each section is derived as follows:

$$H_k(z) = \frac{n_k(b_{0k} + b_{1k}z^{-1} + b_{2k}z^{-2})}{1 + a_{1k}z^{-1} + a_{2k}z^{-2}} \cdot \frac{1}{n_k}. \quad (10)$$

C. Gain Balancing

Using (4) and (10), a stochastic gammatone filter can be designed as a straightforward implementation. However, a very small value of the gain, G (e.g., 6.795×10^{-5} at $f_c = 5$ kHz

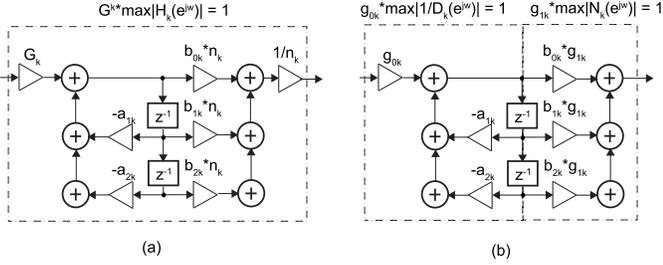


Fig. 7. Second-order sections based on the (a) GGB technique and (b) LGB technique.

TABLE I

SUMMARY OF PARAMETERS FOR GGB AND LGB IN STOCHASTIC GAMMATONE FILTERS AT $f_c = 5$ kHz AND $f_s = 20$ kHz

k	n_k	G_k	g_{0k}	g_{1k}
1	0.125	0.036	0.205	0.174
2	0.5	0.103	0.205	0.500
3	1	0.180	0.205	0.877
4	0.5	0.103	0.205	0.500

and $f_s = 20$ kHz), needs to be represented, causing a very long stochastic bit and hence low speed and large energy dissipation in hardware. To avoid using the very small value of the gain, a globally gain-balancing (GGB) technique is presented. In GGB, an input signal is scaled at each section as shown in Fig. 7(a), while a multiplication with G as shown in Fig. 3 is removed. The gain at each section, G_k , is determined based on the L_∞ norm of $H_k(e^{j\omega})$ as follows:

$$G_k = \frac{1}{\max|H_k(e^{j\omega})|}. \quad (11)$$

Using (11), the transfer function of the gammatone filter based on GGB is derived as follows:

$$H(z) = \prod_{k=1}^4 G_k H_k(z). \quad (12)$$

In addition, G_k is locally distributed to a feedback gain, g_{0k} , and a feedforward gain, g_{1k} , at each section as shown in Fig. 7(b). In the locally gain-balancing (LGB) technique, g_{0k} is first determined based on the L_∞ norm of $1/D_k(e^{j\omega})$ as follows:

$$g_{0k} = \frac{1}{\max|1/D_k(e^{j\omega})|} = \frac{G_k}{g_{1k}}. \quad (13)$$

Then, g_{1k} is determined. Using (13), the transfer function of the gammatone filter based on LGB is derived as follows:

$$H(z) = \prod_{k=1}^4 g_{0k} \frac{g_{1k}(b_{0k} + b_{1k}z^{-1} + b_{2k}z^{-2})}{1 + a_{1k}z^{-1} + a_{2k}z^{-2}}. \quad (14)$$

Parameters of GGB and LGB are summarized in Table I. As the gain values based on GGB and LGB are larger than the original gain, G , the number of stochastic bits can be reduced in comparison with the straightforward implementation, while maintaining the accuracy. The magnitude responses of the stochastic gammatone filters are simulated in the next section.

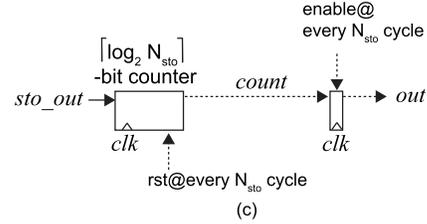
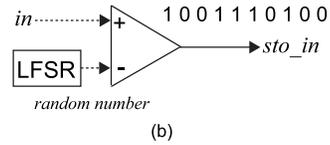
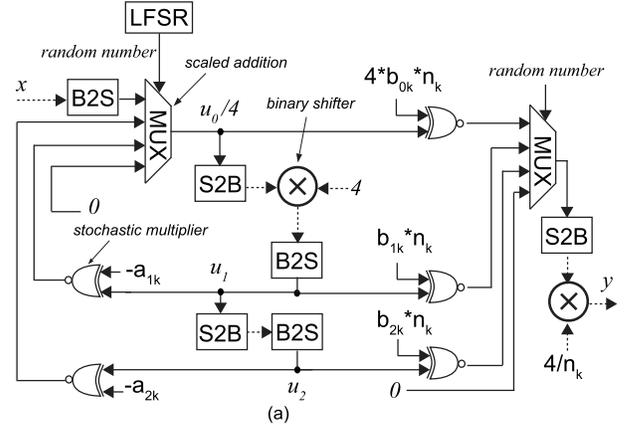


Fig. 8. Second-order IIR filter based on stochastic computation in bipolar coding. (a) Overall structure using normalized coefficients. (b) B2S converter. (c) S2B converter.

IV. CIRCUIT IMPLEMENTATION

A. Purely Stochastic Design

Fig. 8(a) shows a block diagram of a second-order IIR filter based on stochastic computation in bipolar coding. The stochastic IIR filter is designed based on [23]. In the stochastic IIR filter, multiplications are realized using XNOR gates and additions are realized using multiplexors. The input signal in binary coding is converted to a stochastic bit stream using a binary-to-stochastic (B2S) converter shown in Fig. 8(b), where the stochastic bit length is N_{sto} (the number of stochastic bits to represent a real value). In bipolar coding, the input signal can represent a $\lceil \log_2(N_{sto}/2) \rceil$ -bit signed number. The B2S is designed using a linear feedback shift register (LFSR) and a digital comparator. Note that each B2S exploits a different LFSR to reduce correlations between stochastic bit streams.

Delay elements of the second-order IIR filter are designed using stochastic-to-binary (S2B) converters shown in Fig. 8(c). The S2B is designed using a $\lceil \log_2 N_{sto} \rceil$ -bit counter and a $\lceil \log_2 N_{sto} \rceil$ -bit flip-flop. Let us explain the signal transitions in S2B shown in Fig. 9. During the first $(N_{sto}-1)$ clock cycles, the counter operates to count 1s of the stochastic bit stream. Then, in the last one clock cycle, the output of the counter is stored in the flip-flop. Concurrently, the counter is reset. Hence, the total clock cycle is N_{sto} for a one-cycle operation of digital IIR filters.

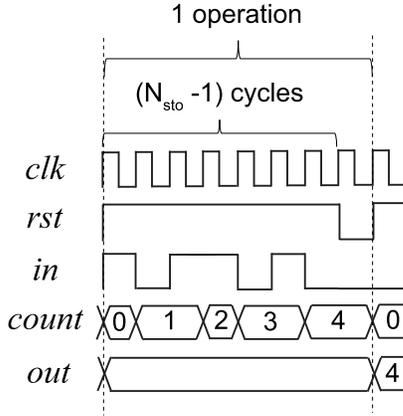


Fig. 9. Example of signal transitions in S2B with $N_{sto} = 2^3$.

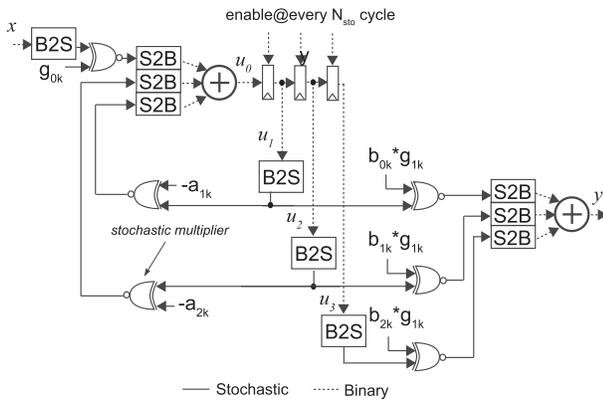


Fig. 10. Second-order IIR filter based on stochastic/binary hybrid computation and LGB, where only multiplications are realized based on stochastic bipolar coding.

As an output signal of the addition is scaled down due to the scaled adder, the output signal after the S2B is scaled up in binary domain based on binary multiplication. For simple hardware, the binary multiplication is designed using a binary shifter because the scaling factor is the power of two. The output value, y , is calculated as follows:

$$y \approx ((4 \cdot b_{0k} \cdot n_k) \cdot (u_0/4) + (b_{1k} \cdot n_k) \cdot u_1 + (b_{2k} \cdot n_k) \cdot u_2) / n_k. \quad (15)$$

The internal value, u_0 , is calculated as follows:

$$u_0 \approx x - a_{1k} \cdot u_1 - a_{2k} \cdot u_2. \quad (16)$$

B. Stochastic/Binary Hybrid Design

The purely stochastic implementation suffers from low computation accuracy due to the stochastic adders, which will be discussed in Section IV-C. To improve the accuracy, the stochastic/binary hybrid filter in bipolar coding is presented as described in Fig. 10. The IIR filter is designed based on LGB, where additions are realized in binary domain instead of stochastic domain. The hybrid computation can improve computation accuracy with a small area overhead [25] compared with an implementation based on only stochastic

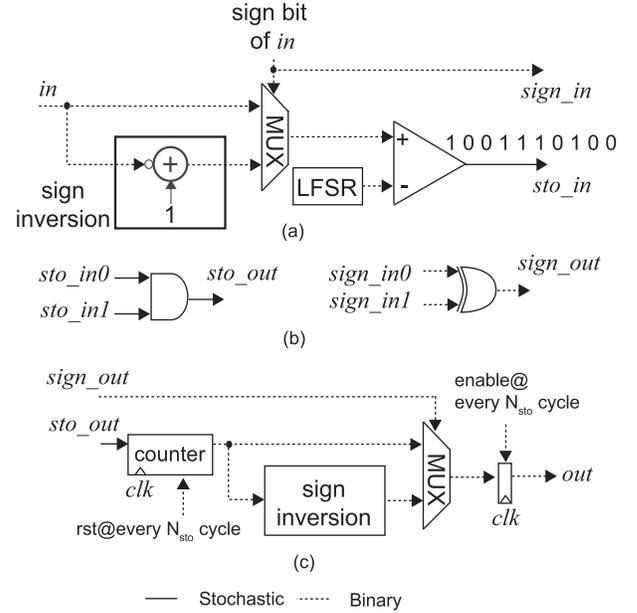


Fig. 11. Circuit components in stochastic/binary hybrid computation with unipolar coding. (a) B2S converter. (b) Multiplier. (c) S2B converter.

computation. There are four internal signals: u_0 , u_1 , u_2 , and u_3 . The internal signal, u_0 , is calculated as follows:

$$u_0 \approx g_{0k} \cdot x - a_{1k} \cdot u_1 - a_{2k} \cdot u_2. \quad (17)$$

The output signal, y , is calculated as follows:

$$y \approx g_{1k}(b_{0k} \cdot u_1 + b_{1k} \cdot u_2 + b_{2k} \cdot u_3). \quad (18)$$

The stochastic/binary hybrid filter is also designed in unipolar coding. Unipolar coding can reduce N_{sto} in comparison with bipolar coding at a similar computation accuracy when only positive values are used. In contrast, it requires a sign bit to represent negative values unlike bipolar coding. Fig. 11 shows circuit components for the stochastic/binary hybrid filter in unipolar coding. In unipolar coding, an input signal is converted to a stochastic bit with a sign bit for representing negative values as shown in Fig. 11(a). The input signal is first determined whether it is positive or negative. If it is negative, then it is converted to a positive value with a sign bit of “1.” In the multiplication shown in Fig. 11(b), a two-input XOR gate and a two-input AND gate are used for the sign calculation and the multiplication, respectively. In the S2B converter shown in Fig. 11(c), the number of “1s” of the stochastic bit stream is first counted and then converted to the negative value, if the sign bit is “1.”

C. Magnitude Responses

The gammatone filters based on stochastic computation are designed and evaluated using MATLAB, where f_c is 5 kHz and f_s is 20 kHz. Fig. 12(a) shows magnitude responses of gammatone filters in bipolar coding, where N_{sto} is 2^{10} . The magnitudes are obtained using a sinusoidal wave as an input signal. Based on the straightforward implementation, the dynamic range is just 1.35 dB, showing a failure operation as gammatone filtering. Note that the dynamic range is used as a ratio of the maximum to minimum magnitude in this paper.

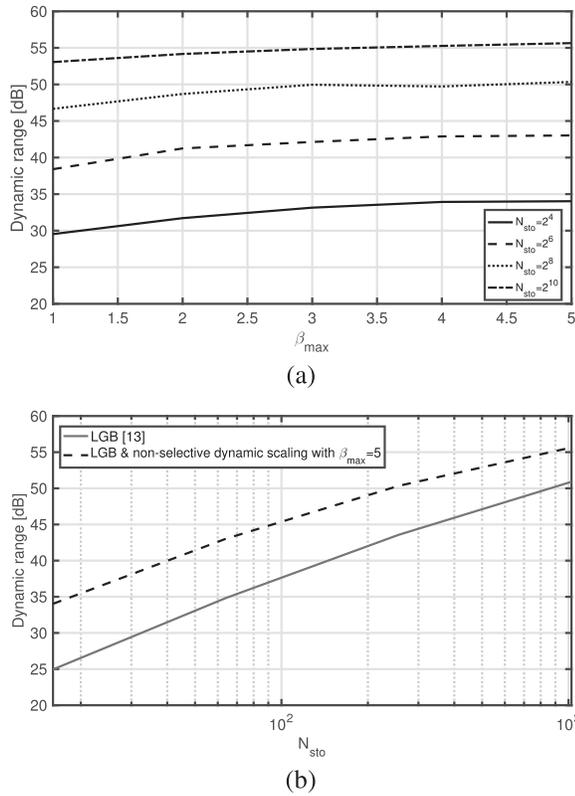


Fig. 12. Magnitude responses of gammatone filters, where N_{sto} is 2^{10} in (a) purely stochastic design with bipolar coding and (b) LGB technique.

It is because a small value of G reduces the computation accuracy. In contrast, using the GGB and the LGB techniques, the dynamic ranges are increased to 5.60 and 17.39 dB, respectively.

Fig. 12(b) shows magnitude responses of gammatone filters based on the LGB technique, where N_{sto} is 2^{10} . The filters are also designed based on stochastic/binary hybrid computation. In the purely stochastic design, all the B2Ss exploit different LFSRs in order to remove the correlations of stochastic bit streams. In the hybrid design, two different LFSRs are used in total: one is shared for input and internal signals and the other one is shared for coefficient signals. It is because the correlations occur only in the stochastic multipliers by removing the stochastic adders. Using the hybrid computation, the dynamic ranges are increased to 29.62 dB in bipolar coding and 50.90 dB in unipolar coding.

To evaluate the hardware complexity of unipolar coding, the stochastic/binary hybrid gammatone filters in bipolar and unipolar coding are designed and synthesized using TSMC 65-nm CMOS technology as summarized in Table II. The two different unipolar filters that include different S2Bs are designed. The first one uses the S2B as shown in Fig. 11(c), and the second one adds an extra flip-flop to *sign_out* of the S2B in order to reduce the worst case delay. The area overheads of the unipolar filters are around 80% in comparison with the bipolar filter. By adding the extra FF to the S2B, the delay overhead is reduced to around 8% in comparison with that without extra FF. The second unipolar filter is useful for high-speed applications, but the first one is chosen for low-complexity hardware in this paper.

TABLE II
PERFORMANCE COMPARISONS OF STOCHASTIC/BINARY HYBRID
GAMMATONE FILTERS IN BIPOLAR AND UNIPOLAR CODING
WITH $N_{\text{STO}} = 2^{10}$ USING TSMC 65-nm
CMOS TECHNOLOGY

	Bipolar	Unipolar	
		w/o extra FF	1 extra FF in S2B
Dynamic range [dB]	29.62	50.90	
Worst-case delay [ns]	1.11	1.99	1.20
Area [μm^2]	10,923	17,163	17,351

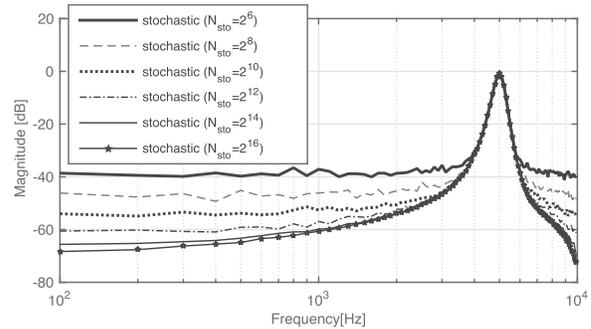


Fig. 13. Magnitude responses versus N_{sto} in the stochastic gammatone filter based on the hybrid computation in unipolar coding.

The magnitude responses versus N_{sto} in the stochastic/binary hybrid gammatone filter based on unipolar coding and the LGB are summarized in Fig. 13. The dynamic range is larger as N_{sto} is larger due to higher computation accuracy. Based on the simulation results, the stochastic/binary hybrid gammatone filter requires long stochastic bits (e.g., $N_{\text{sto}} = 2^{10}$) to realize large dynamic ranges, causing slow speed and large energy consumptions. In the next section, dynamic scaling techniques are presented in order to reduce the length of the stochastic bit stream while maintaining large dynamic ranges.

V. DYNAMIC SCALING

In stochastic computation, small values require long stochastic bits to represent. For example, when 0.0001 is represented in stochastic unipolar coding, at least a 10000-bit stream is required, where only one bit is “1” in the bit stream. To avoid using small values in stochastic computation, two dynamic scaling techniques are presented: nonselective and selective. Note that this section deals with the stochastic/binary hybrid gammatone filter in unipolar coding.

A. Nonselective Dynamic Scaling for Input and Internal Signals

The proposed nonselective dynamic scaling is illustrated as shown in Fig. 14. In the nonselective dynamic scaling, a binary signal is scaled up depending on the value of the binary signal and then converted into a stochastic bit stream. After that, the stochastic bit is converted back to a binary signal, which is then scaled down. Note that the nonselective dynamic scaling is applied to an input signal, x , and internal signals, such as u_0 , while the coefficient signals are constant at each second-order section.

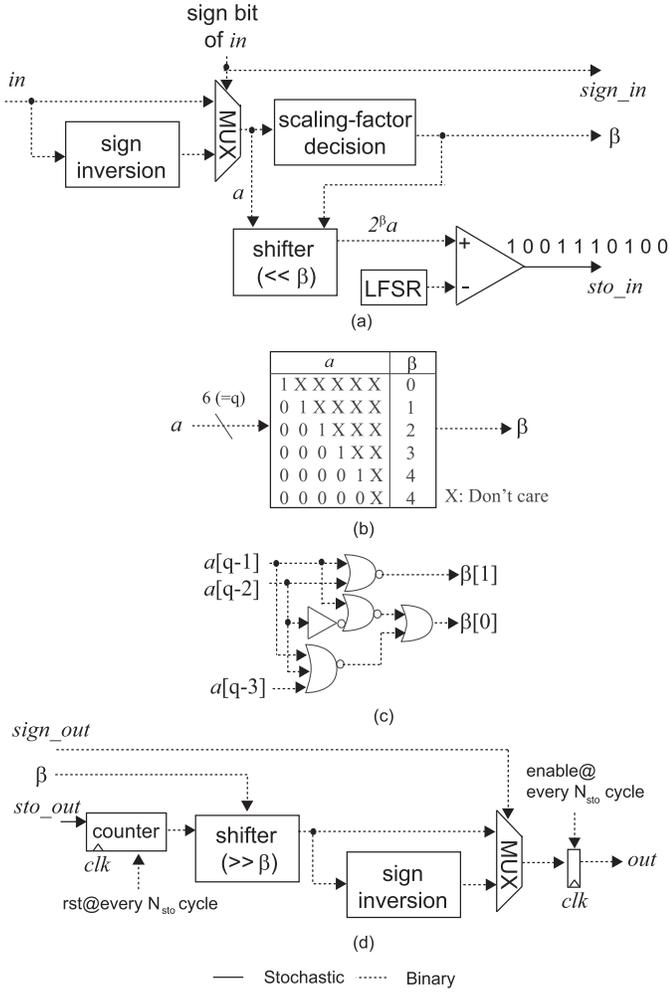


Fig. 14. Nonselective dynamic scaling. (a) B2S converter. (b) General structure of a scaling-factor decision block with $q = 6$ and $\beta_{max} = 4$. (c) Simplified scaling-factor decision block with $\beta_{max} = 3$. (d) S2B converter.

Fig. 14(a) shows a B2S converter with the nonselective dynamic scaling. The converter is the extension of that described in Fig. 11(a). The value of the binary input signal, a , is detected using the scaling-factor decision block. Depending on a , a scaling factor, β , is determined as follows:

$$\beta = \begin{cases} \lfloor \log_2 \lfloor (1/a) \rfloor \rfloor, & (\text{if } \log_2 \lfloor (1/a) \rfloor < \beta_{max}) \\ \beta_{max}, & (\text{otherwise}) \end{cases} \quad (19)$$

where β_{max} is the maximum value of β .

The scaling-factor decision block corresponding to (19) is described in Fig. 14(b). It is designed using a table lookup with *don't care*. Suppose that the binary signal, a , is 6 ($= q$) bits and β_{max} is 4 in this example. The lookup table includes six columns, where the last two columns are redundant. For example, the first column means that a is equal to or more than 0.5 and the second column means that a is equal to or more than 0.25. As a is dynamically scaled up, the effective bits can be extended from q to $(q + \beta_{max})$ at most in stochastic domain. When β_{max} is 3, the scaling-factor decision block is simplified as shown in Fig. 14(c).

After the scaling-factor decision operation, a is scaled up to $(2^\beta \cdot a)$ using the shifter with β and is then converted

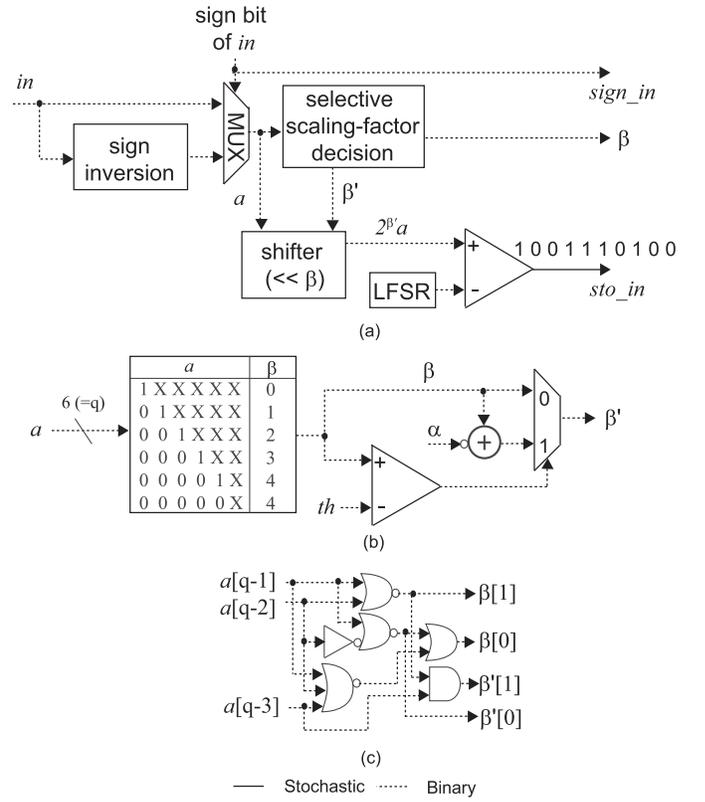


Fig. 15. Selective dynamic scaling. (a) B2S converter. (b) General structure of the selective scaling-factor decision block. (c) Simplified selective scaling-factor decision block with $\beta_{max} = th = \alpha = 3$.

to a stochastic bit. The probability of the stochastic bit is $P_{2^{\beta \cdot a}}$. Hence, there are three outputs in the B2S converter with the nonselective dynamic scaling: a stochastic bit, a sign bit, and β . The multiplication operates as well as that in Fig. 11(b). Fig. 14(d) shows an S2B converter with the nonselective dynamic scaling. The converter is the extension of that described in Fig. 11(c). First, the stochastic bit is converted back to a binary signal. As the binary signal is scaled up in the B2S converter, it is scaled down using the shifter with β . As a result, the probabilities of stochastic bit streams are mostly larger than 0.5, reducing the length of the stochastic bit while maintaining the computation accuracy. The internal signal, u_0 , and the output signal, y , at each section, are determined by (17) and (18), respectively.

B. Selective Dynamic Scaling for Internal Signals

In the selective dynamic scaling, the scaling factor is determined by a value of a binary input signal and a threshold function. Fig. 15(a) shows a B2S converter with the selective dynamic scaling. Note that the selective dynamic scaling is applied to only internal signals while the nonselective dynamic scaling is applied to an input signal, x , at each second-order section. The reason will be discussed in Section VI-A. In the selective dynamic scaling, first, β is determined in (19). Then, the scaling factor in the selective dynamic scaling, β' , is determined as follows:

$$\beta' = \begin{cases} \beta, & (\text{if } \beta < th) \\ \beta - \alpha, & (\text{otherwise}) \end{cases} \quad (20)$$

where th and α are parameters to control β' . Note that α is less than or equal to β_{\max} . The threshold function is a nonlinear function that is not usually used in linear filters, such as finite-impulse response and IIR filters. The nonlinear effects improve the dynamic range that will be shown in Section VI-A.

Fig. 15(b) shows the general structure of the selective scaling-factor decision block with 6 ($=q$) bits and $\beta_{\max} = 4$, where the block is corresponding to (20). Fig. 15(c) shows the simplified selective scaling-factor decision block, where β_{\max} , th , and α are three. After the selective scaling-factor decision operation, a is scaled up to $(2^{\beta'} \cdot a)$ using the shifter with β' , if β is less than the threshold value, th . Otherwise, a is not scaled in this case because β_{\max} and α are the same. The B2S converter is the same as that with the nonselective dynamic scaling. In the selective dynamic scaling, the internal signal at each second-order section, u_0 , is updated from (17) and is described as follows:

$$u_0 \approx g_{0k} \cdot x - (\beta'_{u1} \cdot a_{1k} \cdot u_1) / \beta_{u1} - (\beta'_{u2} \cdot a_{2k} \cdot u_2) / \beta_{u2} \quad (21)$$

where β_{u1} and β'_{u1} are scaling factors for the internal signal, u_1 , and β_{u2} and β'_{u2} are scaling factors for the internal signal, u_2 . The output signal at each section, y , is also updated as follows:

$$y \approx g_{1k} ((\beta'_{u1} \cdot b_{0k} \cdot u_1) / \beta_{u1} + (\beta'_{u2} \cdot b_{1k} \cdot u_2) / \beta_{u2} + (\beta'_{u3} \cdot b_{2k} \cdot u_3) / \beta_{u3}) \quad (22)$$

where β_{u3} and β'_{u3} are scaling factors for the internal signal, u_3 .

VI. EVALUATION

A. Dynamic Range of Stochastic Gammatone Filters

The dynamic ranges of magnitude responses of the stochastic gammatone filters are evaluated using MATLAB, where the filter parameters are used in Fig. 4. The magnitudes are obtained using a sinusoidal wave as an input signal. The input and internal signals are represented by 11 bits, and the coefficient signals are represented by $\lceil \log_2 N_{\text{sto}} \rceil$ bits. These signals are converted to stochastic bit streams using $\lceil \log_2 N_{\text{sto}} \rceil$ -bit LFSRs and comparators. There are two LFSRs used in total, where an LFSR is shared for the input and the internal signals and the other is shared for the coefficient signals. Again note that N_{sto} is the number of clock cycles for a one-cycle operation of digital filters, and the dynamic range is used as a ratio of the maximum to minimum magnitude.

Fig. 16(a) shows dynamic ranges versus β_{\max} with the nonselective dynamic scaling. When β_{\max} is large, the dynamic ranges are large, because a large β_{\max} can scale up small values of binary signals to around 0.5 in most cases. Fig. 16(b) shows dynamic ranges versus N_{sto} . The proposed gammatone filter with $\beta_{\max} = 5$ is compared with the stochastic gammatone filter previously published in [13]. The dynamic ranges of the proposed filter are increased compared with the previous design. In addition, the nonselective dynamic scaling is more effective when N_{sto} is smaller. As a result, the dynamic range is increased to 34.02 from 24.99 [13] with $N_{\text{sto}} = 2^4$.

As opposed to the nonselective dynamic scaling, the selective dynamic scaling is applied to only internal signals as

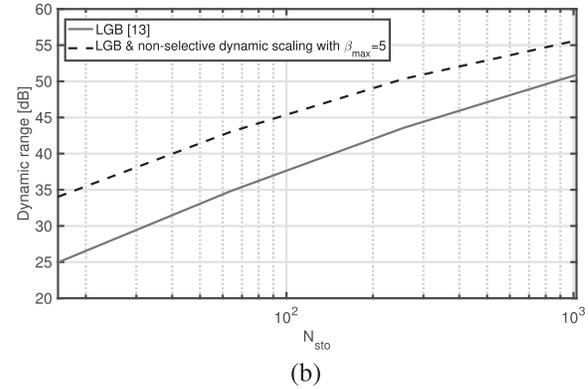
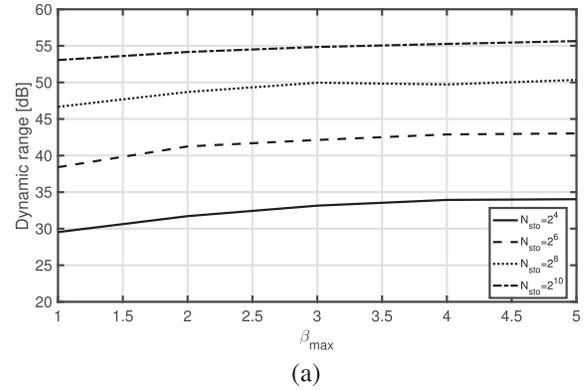


Fig. 16. Dynamic ranges of magnitude responses of the stochastic gammatone filters with nonselective dynamic scaling. (a) Dynamic ranges versus β_{\max} . (b) Comparison with LGB [13].

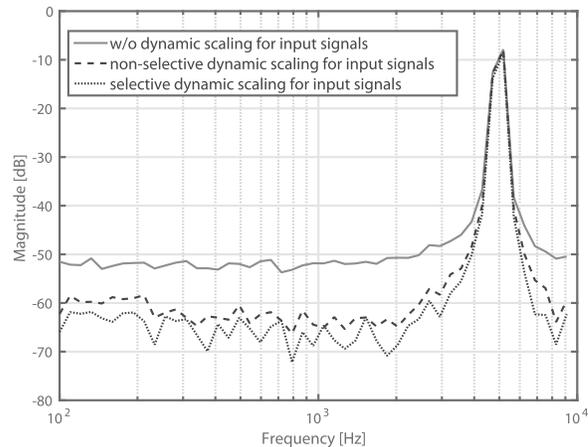


Fig. 17. Effects of the selective dynamic scaling for input signals in the stochastic gammatone filters at $N_{\text{sto}} = 2^4$ in the case of $\beta_{\max} = \text{th} = \alpha = 3$. For internal signals, the selective dynamic scaling is used for all the three cases.

described in Section V-B. To explain the reason clearly, the effects of the selective dynamic scaling for input signals are simulated with $N_{\text{sto}} = 2^4$ as shown in Fig. 17. There are three cases for input signals: no dynamic scaling, the nonselective dynamic scaling ($\beta_{\max} = 3$), and the selective dynamic scaling ($\beta_{\max} = \text{th} = \alpha = 3$). In all cases, the selective dynamic scaling is applied to internal signals with $\beta_{\max} = \text{th} = \alpha = 3$. As shown in Fig. 17, the dynamic ranges of the magnitude responses are increased, thanks to either

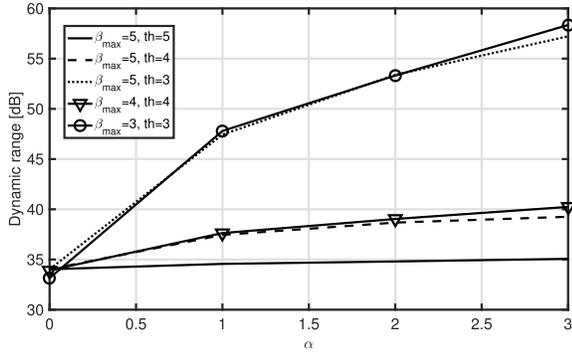


Fig. 18. Dynamic ranges of magnitude responses in the stochastic gammatone filters with selective dynamic scaling at $N_{sto} = 2^4$.

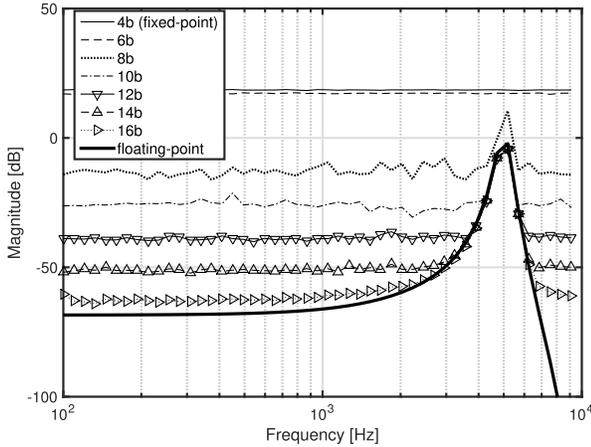


Fig. 19. Magnitude responses of fixed-point gammatone filters, where the bit width including a sign bit ranges from 4 to 16.

nonselective or selective dynamic scaling in comparison with that without dynamic scaling. In contrast, the dynamic ranges between the two dynamic scaling techniques are almost the same, while the selective dynamic scaling technique requires more complicated functions as described in Fig. 15. Hence, the selective dynamic scaling is applied to only internal signals, while the nonselective dynamic scaling is applied to input signals in this paper.

Fig. 18 shows dynamic ranges versus α with the selective dynamic scaling. When α is large, the dynamic ranges are large in all cases. In addition, the dynamic ranges heavily depend on th . The dynamic range reaches to 58.55 dB when β_{max} , th , and α are three with $N_{sto} = 2^4$.

B. Performance Comparisons

The proposed two gammatone filters with the nonselective and selective dynamic scaling are designed using Verilog-HDL, where the filter parameters are used in Fig. 4. For performance comparisons, the stochastic gammatone filter presented in [13] and fixed-point gammatone filters are also designed. The fixed-point gammatone filters are designed in cascaded form as shown in Fig. 3 as well as the stochastic filters. In addition, the GGB technique is applied to optimize the filter gains.

Fig. 19 shows magnitude responses of fixed-point gammatone filters, where the bit width including a sign bit ranges

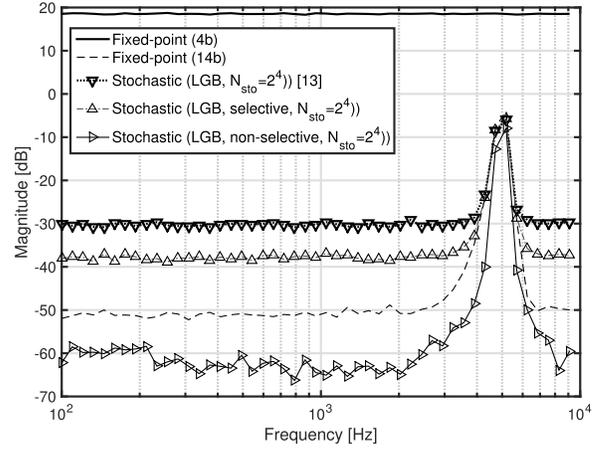


Fig. 20. Comparisons between fixed-point and stochastic gammatone filters in terms of magnitude responses.

TABLE III
SNR OF FIXED-POINT AND STOCHASTIC GAMMATONE FILTERS

f_{in}	7 kHz	8 kHz	9 kHz
Stochastic (selective, $N_{sto} = 2^4$)	-2.8008	-14.9484	-44.3930
Fixed-point (10-bit)	-46.8962	-77.8980	-108.9870
(12-bit)	-34.8712	-59.8204	-98.2182
(14-bit)	-32.0216	-55.5364	-88.2472
(16-bit)	-15.2052	-33.3320	-70.7290
(18-bit)	-1.5982	-22.5682	-61.6066

from 4 to 16. The magnitude responses are obtained using a sinusoidal wave as an input signal. In the fixed-point design, three bits are used for integer to represent the coefficients. In case of the bit widths of 4 and 6, there are no filter responses due to too small bit widths.

Fig. 20 shows comparisons of magnitude responses of the gammatone filters. The 14-bit fixed-point filter achieves a dynamic range of 48.24 dB. The stochastic gammatone filters with LGB and $N_{sto} = 2^4$ achieve 33.15 and 58.35 dB, respectively, in the case of the nonselective and the selective dynamic scaling techniques. Note that the nonselective dynamic scaling technique uses $\beta_{max} = 3$ and the selective dynamic scaling technique uses $\beta_{max} = th = \alpha = 3$.

Table III summarizes signal-to-noise ratios (SNRs) of the fixed-point and stochastic gammatone filters, where f_{in} is a frequency of input signals. The SNR is defined based on [17] as follows:

$$SNR = 10 \cdot \log_{10} \left(\frac{\sum |y_{float}|^2}{\sum |y_{float} - y_{comp}|^2} \right) \quad (23)$$

where y_{float} is the output signal of the floating-point gammatone filter and y_{comp} is the output signal of the fixed-point or the stochastic gammatone filter with $N_{sto} = 2^4$ and the selective dynamic scaling. The SNR values are reasonably small as the output signals are filtered. In most cases, the proposed stochastic gammatone filter shows larger SNRs than the fixed-point filters.

For hardware evaluation in the case of high-speed applications, the gammatone filters are synthesized using Synopsys design compiler on TSMC 65-nm CMOS Technology. The power consumptions are evaluated using Synopsys

TABLE IV
PERFORMANCE COMPARISONS OF GAMMATONE FILTERS USING TSMC 65-nm CMOS TECHNOLOGY

Design style	Baseline		[13]	This work	
	Fixed-point		(LGB)	Stochastic/binary	
	(4-bit)	(14-bit)		(LGB and non-selective dynamic scaling $\beta_{max}=3$)	(LGB and selective dynamic scaling $\beta_{max}=th=\alpha=3$)
N_{sto}	-	-	1024	256	16
Dynamic range [dB]	0	48.24	50.90	49.96	58.35
Area [μm^2]	6.641	55.752	17,163	12,418	5,156
Total power dissipation@100 MHz [mW] (dynamic power) (static power)	0.179	6.409	0.968	0.777	0.313
	0.140	6.069	0.882	0.714	0.286
	0.039	0.341	0.087	0.063	0.026
Energy dissipation [pJ]	1.79	64.1	9312.3	1989.1	50.1
Worst-case delay [ns]	1.90	3.89	1.99	1.61	0.96
Latency [ns]	7.60	15.56	8151.04	1648.64	61.44

power compiler. Table IV summarizes the performance of the gammatone filters with a dynamic range of around 50 dB, other than the 4-bit fixed-point filter. Using the selective dynamic scaling technique, the proposed gammatone filter reduces N_{sto} to 2^4 from 2^{10} of the previous stochastic gammatone filter [13] while maintaining the dynamic range. The area reductions of the previous and the proposed nonselective and selective stochastic filters are 69.2%, 77.7%, and 90.7%, respectively, in comparison with the 14-bit fixed-point gammatone filter, thanks to eliminating area-hungry multipliers. In addition, the proposed filter with the selective dynamic scaling reduces the area by 70% compared with the previous stochastic filter because the areas of the B2S and the S2B converters depend on N_{sto} .

The power dissipations obtained at a frequency of 100 MHz are used to evaluate the energy dissipations. The power dissipations of the stochastic gammatone filters are reduced compared with that of the 14-bit fixed-point design because of the small areas, while the stochastic gammatone filters require N_{sto} clock cycles for a one-cycle operation of the fixed-point filter. Hence, the previous stochastic gammatone filter consumes around $145\times$ energy dissipation of that of the fixed-point filter. In contrast, the energy dissipation of the proposed filter with the selective dynamic scaling is 78.1% of that of the fixed-point filter because of a small N_{sto} . The latencies are calculated by multiplications of “worst case delay,” N_{sto} , and four (the number of cascaded sections). The stochastic gammatone filter with the selective dynamic scaling exhibits around four times larger latency than the 14-bit fixed-point design.

C. Power Dissipation at a Sampling Frequency of 48 kHz

In this section, the power dissipations are evaluated for lower speed applications than that described in the previous section. The gammatone filters can be used at a sampling frequency of 16 or 48 kHz for auditory signal processing as voice signal processing often uses 16 kHz, such as VoIP, and audio signal processing often uses 48 kHz, such as DVD [26]. Fig. 21 shows the power dissipations of gammatone filters operating at a sampling frequency of 48 kHz. A clock frequency of the fixed-point design is 48 kHz, while the proposed stochastic filter with the selective dynamic scaling operates at 768 kHz because of $N_{sto} = 2^4$. In addition, the previous

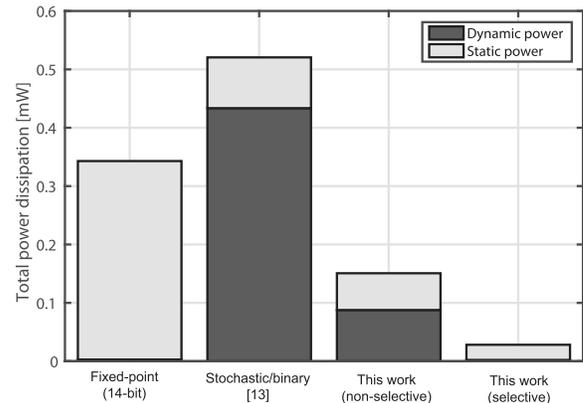


Fig. 21. Power dissipations of gammatone filters operating at a sampling frequency of 48 kHz.

stochastic filter with $N_{sto} = 2^{10}$ operates at 49.152 MHz and the proposed filter based on the nonselective dynamic scaling with $N_{sto} = 2^8$ operates at 12.288 MHz. It means that fixed-point and stochastic gammatone filters operate at the same sampling frequency of 48 kHz.

In such a low-speed case, the static power dissipation dominates the total power dissipation because of low clock frequencies in the fixed-point and the proposed gammatone filters. For example, the ratios between the static and the total power dissipations are 99.1% and 92.2% in the fixed-point and the proposed stochastic filter with the selective dynamic scaling, respectively. As the static power dissipations mostly depend on area, the proposed stochastic filter with the selective dynamic scaling reduces the static power dissipation and the total power dissipation by 92.4% and 91.8%, respectively, in comparison with that of the fixed-point filter. In addition, the proposed filter with the nonselective dynamic scaling reduces the static and the total power dissipations by 81.5% and 56.0%, respectively, in comparison with that of the fixed-point filter.

D. Comparison With Related Work

Fig. 22 shows performance comparisons with analog implementations for a gammatone filter. As the proposed stochastic filter is designed on TSMC 65-nm CMOS technology, the area and the energy dissipations are scaled to $0.18 \mu\text{m}$ used in [10].

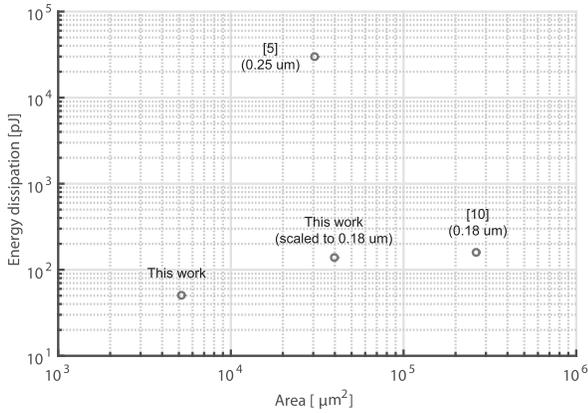


Fig. 22. Performance comparisons with analog implementations of gammatone filters.

Suppose that the gammatone filters are used for analog-mixed speech-recognition systems, such as Fig. 1. In such systems, analog-to-digital converters (ADCs) are required in both analog and stochastic implementations, where the analog implementations need ADCs after gammatone filtering and the stochastic implementations need ADCs before gammatone filtering. Hence, the hardware overheads of ADCs are ignored in the performance comparison. Note that the overheads can be eliminated using analog-to-stochastic converters in the stochastic implementations [27], [28].

The proposed stochastic filter with the selective dynamic scaling achieves a better energy efficiency and smaller area than that of the analog gammatone filter [10]. In [5], the area is smaller than that of the proposed filter while the energy dissipation is significantly larger. Note that the proposed stochastic filter is scalable to CMOS technologies because of the purely digital implementation while the analog implementations suffer from the CMOS scaling. In terms of dynamic ranges, the proposed stochastic filter achieves a dynamic range of around 50 dB as well as the analog implementations.

VII. CONCLUSION

In this paper, the gammatone filters based on stochastic computation have been presented for area/energy-efficient hardware, such as IoT devices. The straightforward implementation of the stochastic gammatone filter designed using the cascaded second-order IIR filter is evaluated that causes the very low dynamic range due to the very small value of the filter gain. To increase the dynamic range, the gain-balancing techniques have been proposed that split the original small gain to multiple larger gains, increasing the dynamic range.

In addition, dynamic scaling techniques are proposed that scales up small values only on stochastic domain, reducing N_{sto} from 2^{10} to 2^4 while maintaining the dynamic range. As a result, the proposed stochastic gammatone filter achieves a high dynamic range of 58.35 dB with $N_{sto} = 2^4$ compared with a low dynamic range of 1.35 dB with $N_{sto} = 2^{10}$ in the straightforward implementation. For performance comparisons, the proposed stochastic gammatone filters are designed using Verilog-HDL and evaluated on TSMC 65-nm CMOS technology. As a result, the proposed filter achieves an area

reduction of 90.7% and an energy reduction of 91.8% in comparison with that of the 14-bit fixed-point gammatone filter at the same sampling frequency and the comparable dynamic range. The proposed stochastic filter achieves a dynamic range of around 50 dB as well as the analog implementations. The 50-dB dynamic range is similar to the floating-point result at a lower frequency than the center frequency as shown in Fig. 2, while the ideal gammatone filter exhibits an over 100-dB dynamic range at the higher frequency. As the audible range of human is from around 0 to over 100 dB, such a large dynamic range would be required, if the gammatone-filter VLSI is designed for the brainware auditory signal processing.

Future works include lowering a supply voltage to achieve a better energy efficiency in a fabricated chip, such as analog implementations, and designing a gammatone filterbank for robust speech-recognition systems.

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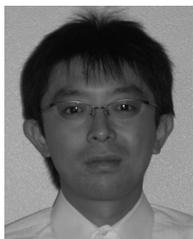


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