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Paper

An area/power-aware 32-channel compressive gammachirp filterbank chip based on hybrid stochastic/binary computation

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Abstract: This paper presents a 32-channel compressive gammachirp filterbank chip based on hybrid stochastic/binary computation for area/power-efficient auditory signal processing. The gammachirp filter well expresses the performance of human auditory peripheral mechanism and can be used for hearing assisting devices and noise robust speech recognition systems. The stochastic gammachirp filters are designed using cascaded digital IIR filters, leading to area-efficient hardware thanks to a simple logic-gate implementation of multiplication. However, the signal variability due to random number sequences used in stochastic computation induces unwanted frequency components at each IIR filter, causing large noise signals at the output of the gammachirp filters. To reduce the noise signals, a fixed random-number-generation (FRNG) technique is introduced that provides the same random number sequence at every operation as opposed to different random number sequences used in a conventional stochastic filter. The FRNG technique mitigates the noise signals and hence increases the filter gains with short lengths of stochastic bit streams. In addition, gain-compression characteristics depending on input acoustic pressures known as human auditory effects are naturally realized by changing the lengths of the stochastic bit streams. The proposed filterbank chip is fabricated using Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS process that achieves 715-2,585 μW with the chip area of 3.2 mm^2, leading to the best power-area product per channel in comparison with conventional analog auditory filterbanks.

Key Words: stochastic logic, gammachirp filter, auditory filter, IIR filter, digital circuit implementation

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1. Introduction

Brainware (brain-inspired) computing and LSI (BLSI) implementations have recently been studied for image recognitions, leading to a significant cognition capability compared to a traditional computation based approach [1, 2]. In brainware auditory signal processing, gammatone filters [3, 4] and gammachirp filters [5–8] are promising techniques for advanced speech communication systems as these filters exhibit similar responses to the impulse responses of basilar membrane. There are several applications, such as cochlear implants [9–12] and noise robust speech recognitions [13–15].

However, the gammachirp filters designed as an extension of the gammatone filters require high computational power because the functions are complicated. The VLSI implementations of the gammatone filters have been studied using analog [9, 10] or digital circuits [11] as the gammatone filters are also complicated. The analog implementations can achieve low-energy dissipation with CMOS scaling issues, while the digital implementations suffer from the hardware complexity due to a large number of multipliers. Recently, stochastic gammatone filters are presented in order to address these issues [12]. In contrast, the hardware implementation of the gammachirp filters has not been presented, to the best of our knowledge.

In this paper, we present an area/power-aware 32-channel compressive gammachirp filterbank chip based on stochastic computation using TSMC 65 nm CMOS general-purpose process. Stochastic computation [16, 17] is a purely-digital implementation technique that represents data as streams of random bits. Stochastic circuits can scale down with the advanced CMOS process, while a power-and-area hungry multiplier used in digital infinite impulse response (IIR) filters is realized using a simple logic gate. Using stochastic computation, the gammachirp filters are designed using a cascaded connection of the stochastic gammatone filters [12] and asymmetric compensation filters, where both filters are designed using cascaded 2nd-order IIR filters. However, the output signals of the stochastic gammachirp filters are with large noise as the noise signals are added at each IIR section due to randomness of stochastic computation. To address the issue, a fixed random-number-generation (FRNG) technique is introduced that mitigates the randomness and hence reduces the noise signals. This technique is similar to [18] that reuses random number sequences stored in a memory, where the hardware implementations are different. Using the FRNG technique, large gains (dynamic ranges) of the gammachirp filters are achieved with short lengths of stochastic bit streams. In addition, gain-compression characteristics depending on input acoustic pressures known as human auditory effects are naturally realized by changing the lengths of the stochastic bit streams. In comparison with the related works [19–21], the proposed chip is the first silicon that realizes both asymmetric characteristic in frequency domain and gain compression depending on input acoustic pressures while achieving the best power-area product per channel.

The rest of the paper is organized as follows. Section 2 shows the design overview of the proposed gammachirp filterbank chip. Section 3 describes the stochastic gammachirp-filter circuits based on the FRNG technique. Section 4 evaluates the proposed chip and compares with related works. Section 5 concludes this paper.

2. Design overview of compressive gammachirp filterbank chip

2.1 Compressive gammachirp filter

Gammatone filters [3, 4] and gammachirp filters [5–8] are promising techniques for advanced speech communication systems as these filters exhibit similar responses to the impulse responses of basilar membrane. As opposed to the gammatone filter, the gammachirp filter is asymmetric, providing a more realistic auditory filtering for models of auditory perception. A gammachirp filter is represented by an impulse response [5] defined as follows:

$$g(t) = at^{M-1}e^{-2\pi b\mathrm{ERB}(f_r)t}\cos(2\pi f_r t + c\ln t + \phi)\ (t > 0), \tag{1}$$

where a is a constant, M is the order of the filter, b is the bandwidth of the filter, f_r (Hz) is the asymptotic frequency of the filter, c is a parameter for the frequency modulation on the chirp rate, and ϕ is the steering phase. In this paper, a is set to 1 and ϕ is set to 0 used [10] and M=4 and

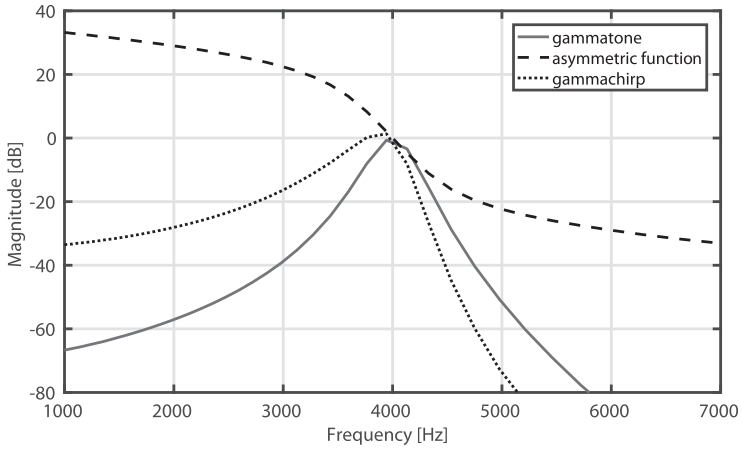

Fig. 1. Frequency responses of a gammachirp filter at f_r=4 kHz, f_s=16 kHz, and c=−2, where gammachirp filters are modeled using gammatone filters and asymmetric compensation filters.

b=1.019 are used in [6]. ERB(f_r) is the equivalent rectangular bandwidth of the auditory filter at f_r, where ERB(f_r) is 24.7+0.108f_r. The frequency response of the gammachirp filter is represented [6] as follows:

$$G_C(f) \approx G_T(f) \cdot H_C(f), \tag{2}$$

where $G_T(f)$ is the frequency response of a gammatone filter [3] and $H_C(f)$ is the frequency response of an asymmetric compensation filter.

The gammatone filter is represented by an impulse response that is the product of a gamma distribution and a sinusoidal tone as follows:

$$g(t) = at^{n-1}e^{-2\pi b\mathrm{ERB}(f_c)t}\cos(2\pi f_c t + \phi)\ (t > 0). \tag{3}$$

The transfer function of the gammatone filter in digital domain, $H(z)$, is described using an 8th-order digital IIR filter as follows:

$$H(z) = \frac{b_0 + b_1 z^{-1} + ... + b_8 z^{-8}}{1 + a_1 z^{-1} + ... + a_8 z^{-8}}, \tag{4}$$

where b_n $(0 \le n \le 8)$ and a_m $(1 \le m \le 8)$ are coefficients. The transfer function is realized by four cascaded IIR filters. The detail of the gammatone filter is described in [12].

The asymmetric compensation filter is designed using a cascaded digital filter defined as follows:

$$H_C(z) = \prod_{k=1}^{N} H_{Ck}(z), \tag{5}$$

where N=4 is used [6]. The digital filter at each section is designed using an IIR filter as follows:

$$H_{Ck}(z) = \frac{(1 - r_k e^{j\varphi_k} z^{-1})(1 - r_k e^{-j\varphi_k} z^{-1})}{(1 - r_k e^{j\phi_k} z^{-1})(1 - r_k e^{-j\phi_k} z^{-1})}, \tag{6}$$

where $r_k = e^{-k \cdot p_1 \cdot 2\pi b\mathrm{ERB}(f_r)/f_s}$, $\phi_k = 2\pi(f_r + p_0^{k-1} \cdot p_2 \cdot c \cdot 2\pi b\mathrm{ERB}(f_r))/f_s$, and $\varphi_k = 2\pi(f_r - p_0^{k-1} \cdot p_2 \cdot c \cdot 2\pi b\mathrm{ERB}(f_r))/f_s$. The parameters of p_0, p_1, and p_2 determined in [8] are used in this paper.

Figure 1 shows the frequency responses of a gammachirp filter at f_r=4 kHz, f_s=16 kHz, and c=−2, where f_s is a sampling frequency. In addition, in case of a compressive gammachirp filters, the gains of the gammachirp filters are compressed when the input acoustic pressures are high as shown in Fig. 2.

2.2 Filterbank design

A system architecture of the 32-channel compressive gammachirp filterbank chip is shown in Fig. 3. The input signal is a signed 11-bit width at the sampling frequency (f_s) = 48 kHz with a control

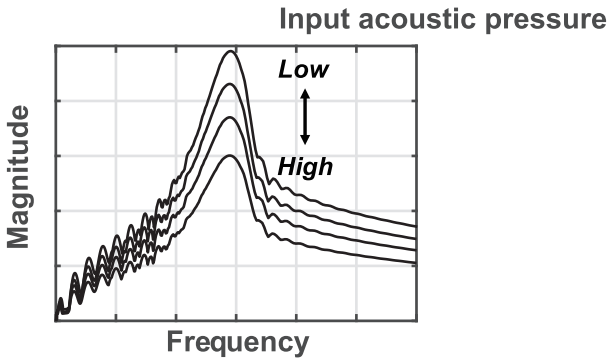

Fig. 2. Example of gain-compression feature depending on input acoustic pressure.

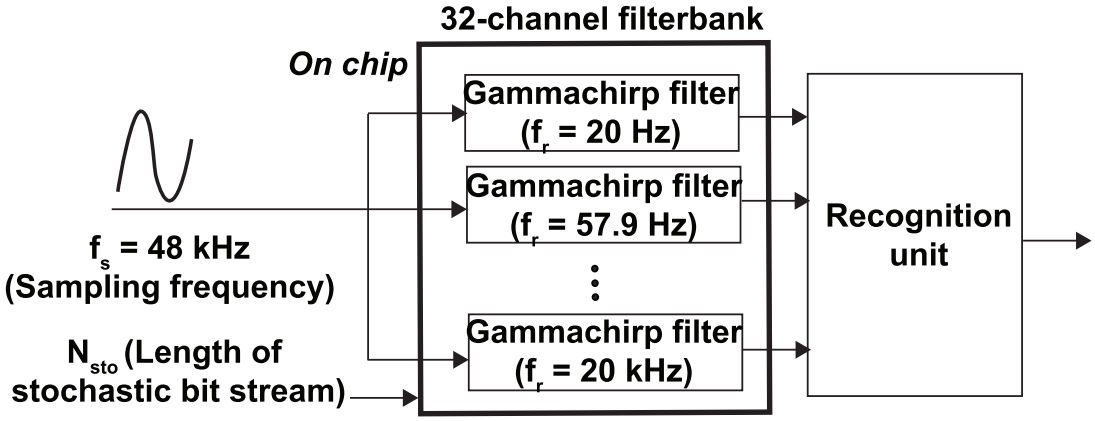

Fig. 3. Architecture of a 32-channel compressive gammachirp filterbank chip with magnitude responses from 20 Hz to 20 kHz.

f_r [Hz]	ERB(f_r)	$ERB_N(f_r)$	f_r [Hz]	ERB(f_r)	$ERB_N(f_r)$
20	26.86	0.77873	2179.67	260.104	21.8757
57.9299	30.9564	2.09729	2546.8	299.754	23.1942
101.641	35.6773	3.41585	2969.89	345.448	24.5128
152.016	41.1177	4.73441	3457.48	398.107	25.8314
210.069	47.3875	6.05297	4019.38	458.793	27.1499
276.971	54.6129	7.37153	4666.94	528.73	28.4685
354.072	62.9397	8.69009	5413.21	609.327	29.787
442.924	72.5358	10.0086	6273.23	702.209	31.1056
545.321	83.5947	11.3272	7264.35	809.25	32.4242
663.326	96.3392	12.6458	8406.54	932.607	33.7427
799.319	111.026	13.9643	9722.84	1074.77	35.0613
956.041	127.952	15.2829	11239.8	1238.6	36.3798
1136.65	147.458	16.6014	12988	1427.4	37.6984
1344.79	169.938	17.92	15002.6	1644.98	39.017
1584.66	195.844	19.2386	17324.4	1895.73	40.3355
1861.1	225.699	20.5571	20000	2184.7	41.6541

Fig. 4. ERB and ERB_number (ERBN) listed above used for the 32-channel stochastic compressive gammachirp filterbank chip.

signal, N_{sto}, that is the length of the stochastic bit streams per operation. The gammachirp filters are represented by the impulse responses with the ERBs, where the asymptotic (center) frequency (f_r) of the gammachirp filters ranges from 20 Hz to 20 kHz. The ERBs corresponding to the frequency range are listed in Fig. 4. The magnitude responses of the filterbank are shown in Fig. 5.

The gammachirp filters are designed using a cascaded connection of 2nd-order IIR filters as shown

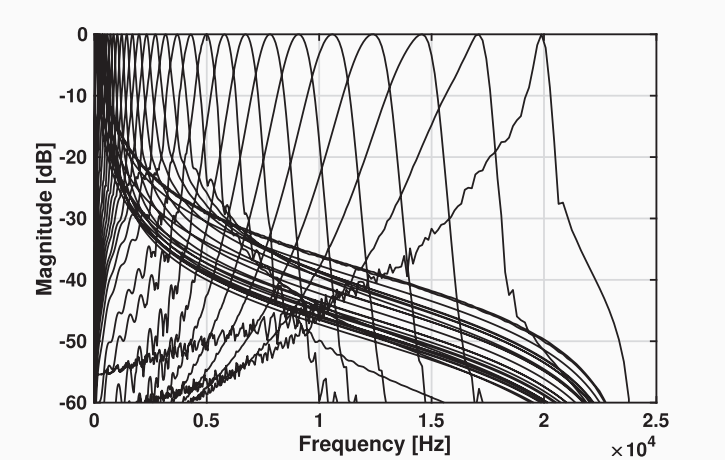

Fig. 5. Magnitude responses of the 32-channel gammachirp filterbank.

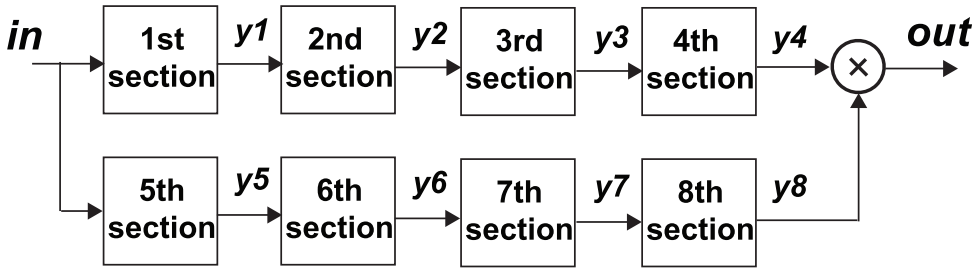

Fig. 6. Gammachirp filter designed using gammatone (top) and asymmetric compensation filters (bottom). Each filter is designed using a four-cascaded 2nd-order IIR filter.

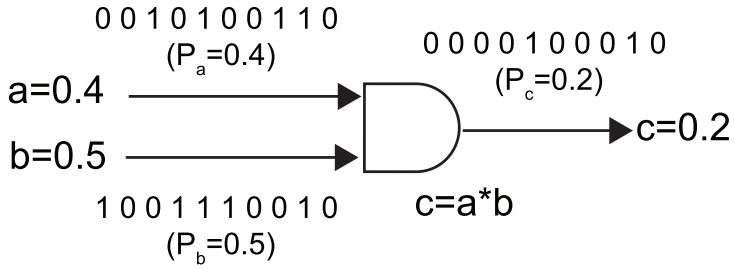

Fig. 7. Multiplier in stochastic computation based on unipolar coding.

in Fig. 6. The asymmetric characteristics of the gammachirp filters are realized by combining the symmetric gammatone filters and asymmetric compensation filters.

3. Stochastic circuit implementation

3.1 Stochastic computation

Stochastic computation has been recently studied for several applications, such as low-density parity-check (LDPC) decoding [22, 23], image processing/recognition [24–27], and digital filters [12, 28–30]. In stochastic computation, information is carried by the frequency of ones in a sequence based on *unipolar* coding or *bipolar* coding. In this paper, unipolar coding is used. A value a is $a = P_a, (0 \leq a \leq 1)$, where the probability of observing a '1' to be P_a =Pr$(a(t) = 1)$ for a sequence of bits, $a(t)$. A multiplier is simply designed using a 2-input AND gate [17] shown in Fig. 7.

3.2 IIR filters based on hybrid stochastic/binary computation

Figure 8 shows a 2nd-order IIR filter based on stochastic/binary hybrid computation in unipolar coding. In the hybrid design, multipliers are designed based on stochastic computation while adders are designed based on binary logic [31]. As unipolar coding represents only positive values, sign bits

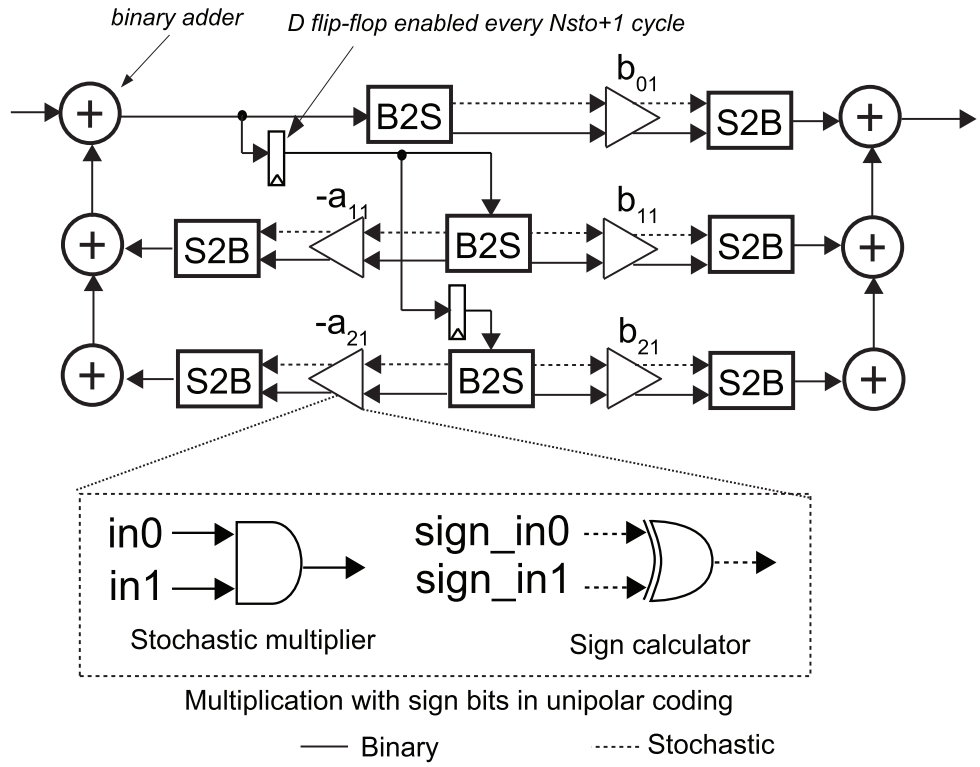

Fig. 8. 2nd-order IIR filter based on stochastic/binary hybrid computation in unipolar coding, where additions are realized in binary domain and multiplications are realized in stochastic domain.

with stochastic bit streams are used to represent negative values. Hence, multiplications are realized using a 2-input AND gate and a 2-input XOR gate in the stochastic IIR filter. The hybrid IIR filter is designed for the gammachirp filters and hence it is hard to compare with other stochastic IIR filters [29–31], directly.

Binary-to-stochastic (B2S) and stochastic-to-binary (S2B) converters are described in Fig. 9. The timing diagrams are shown in Fig. 10. In B2S, firstly, a binary input signal is determined whether it is positive or negative using the sign inversion block. The length of the stochastic bit stream, N_{sto}, is $(N_{cyc}-1)$, where N_{cyc} is the number of cycles for an operation in binary domain. Then, the absolute value of the input signal is compared with random values generated by a linear feedback shift register (LFSR) in order to generate a stochastic bit stream. In addition, a sign bit is generated to represent negative values.

Using stochastic bit streams and sign bits, multiplications are carried out in stochastic domain for N_{sto} cycles. In S2B, the number of 1's in a stochastic bit stream is counted for N_{sto} cycles and is then converted back to a binary signal for a cycle. The binary signal is changed to negative, if the sign bit is "1".

3.3 Fixed random-number generation (FRNG) for reducing noise signals

The stochastic gammachirp filters are designed using the cascaded connection of the stochastic gammatone filters and the asymmetric compensation filters as shown in Fig. 6. In the stochastic IIR filters, there are signal variabilities as random number sequences are used in B2S. The signal variabilities induce unwanted frequency components on signals and hence generate noise signals. As the noise signals are added at each IIR filter, the output signals of the stochastic gammachirp filters are with a large noise at the end.

To reduce the noise signals added at each section, a fixed random-number-generation (FRNG) technique is introduced. This technique is similar to [18] that reuses random number sequences. However, the hardware implementation is different, where the technique in [18] uses a memory that stores the random number sequences generated by software in advance. In the conventional random-

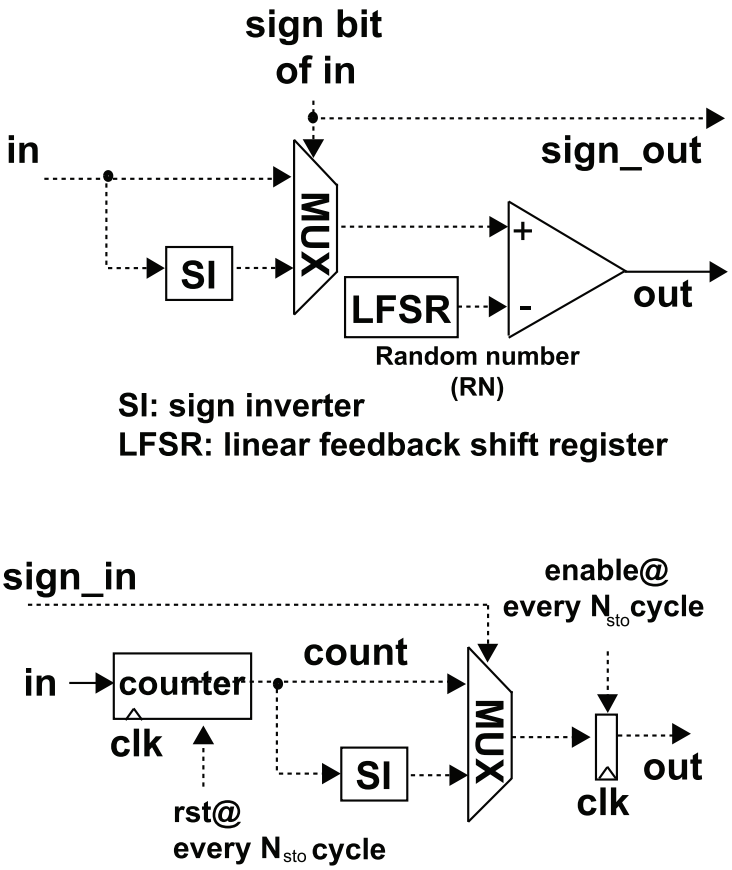

Fig. 9. Stochastic circuit components: binary-to-stochastic (B2S) converter (top) and stochastic-to-binary (S2B) converter (bottom).

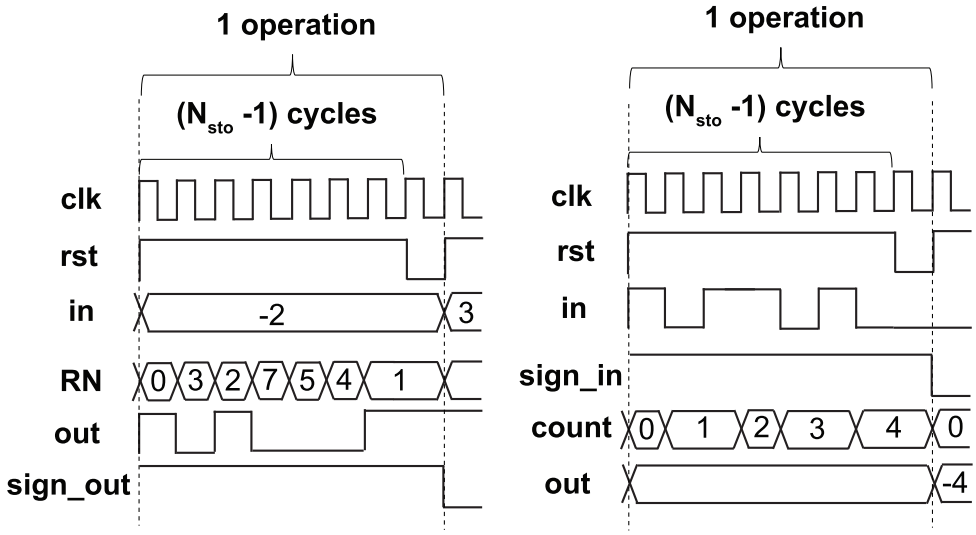

Fig. 10. Example of timing diagrams of B2S (left) and S2B (right) of stochastic 2nd-order IIR filter.

number generation (RNG), random numbers are generated using LFSRs to generate stochastic bit streams. Normally, the repeating cycle of LFSRs is longer than N_{cyc} in stochastic computation because longer cycles tend to exhibit randomness. Hence, at every operation, different random-number sequences are used as shown in Fig. 11(a). However, the randomness induces the noise signals in the stochastic IIR filters.

The FRNG exploits fixed random-number sequences to reduce the randomness as shown in Fig. 11(b). In FRNG, the same random-number sequence is used at every operation. The same

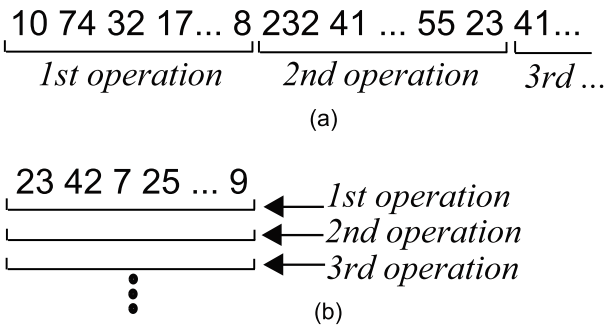

Fig. 11. Random number sequences used in B2S based on (a) conventional random number generation (RNG) and (b) fixed random number generation (FRNG). In FRNG, the same random number sequence is used at every operation.

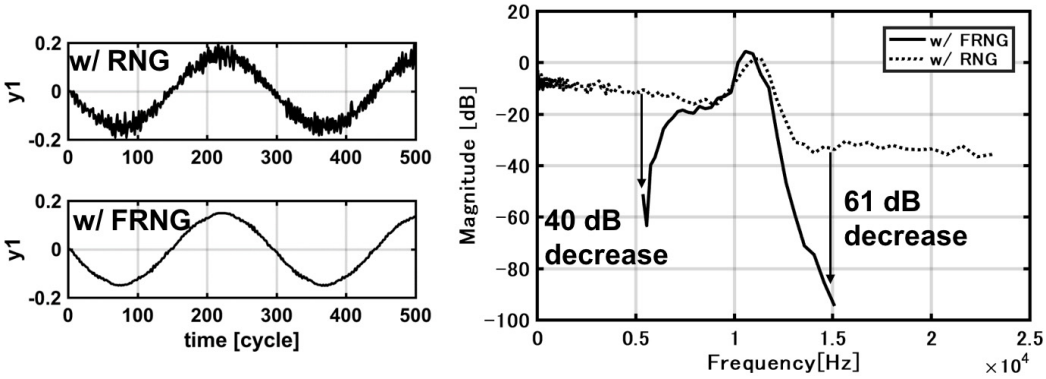

Fig. 12. Output signals of 1st section ($y1$) at f_{in} = 163 Hz (left) and magnitude responses of channel 28 at $N_{sto} = 2^{10} - 1$ (right) using MATLAB simulation.

sequence mitigates the randomness and hence reduces the noise signals in the stochastic IIR filters. The same random-number sequence at every operation can be generated when the bit width of LFSRs is $\log_2 N_{cyc}$, where the repeating cycle is N_{sto} $(= (N_{cyc} - 1))$.

Figure 12 shows the simulated output signal ($y1$) of the 1st section of the filter when an input signal is a sinusoidal wave of a frequency $(f_{In}) = 163$ Hz using MATLAB. In the conventional RNG, the bit widths (n) of the LFSRs are determined with a condition of $((2^n - 1) > N_{sto})$ for sufficient enough bit lengths. However, the random number sequences generated using the LFSRs are different per operation, which cause noisy signals. Hence, the magnitude responses with the conventional RNG exhibit small dynamic ranges. To cope with the issue, the FRNG generates the same random sequence every operation by a condition of $((2^n - 1) = N_{sto})$. The same random sequence reduces the variability of data values between operations, which leads to less noisy signals and higher dynamic ranges (40 dB and 61 dB) increases with $N_{sto} = 2^{10} - 1$ at channel 28 than the conventional RNG.

4. Evaluation

Figure 13 shows the 32-channel stochastic gammachirp filterbank chip using TSMC 65 nm CMOS general-purpose process with the chip area of 3.2 mm^2. The performance is evaluated using the test environment that includes Digilent Genesys 2 FPGA and Keysight N6705B shown in Fig. 14. The fabricated chip operates from VDD = 1.0V to 0.55V at nominal temperature, which exhibits gammachirp filter responses. The clock frequency is $f_s * N_{sto}$, where f_s is 48 kHz and is variable depending on N_{sto}. By changing N_{sto} and the frequency, the gain compressions are realized.

Figure 15 shows the power dissipation vs. N_{sto} of the proposed chip with the supply voltage of 0.55 V. In case of a low clock-frequency region (< 10 MHz), the power dissipations are not strongly reduced by lowering the clock frequency as the total power dissipation is dominated by the static power dissipation. Figure 16 shows energy/sample vs. N_{sto} of the proposed chip with the supply voltage of 0.55V.

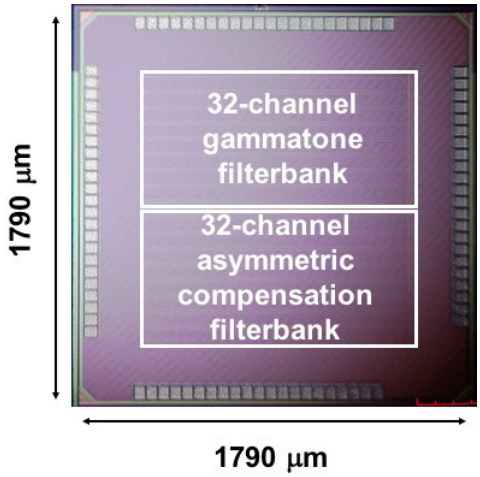

Fig. 13. Photomicrograph of the proposed chip using TSMC 65 nm CMOS process.

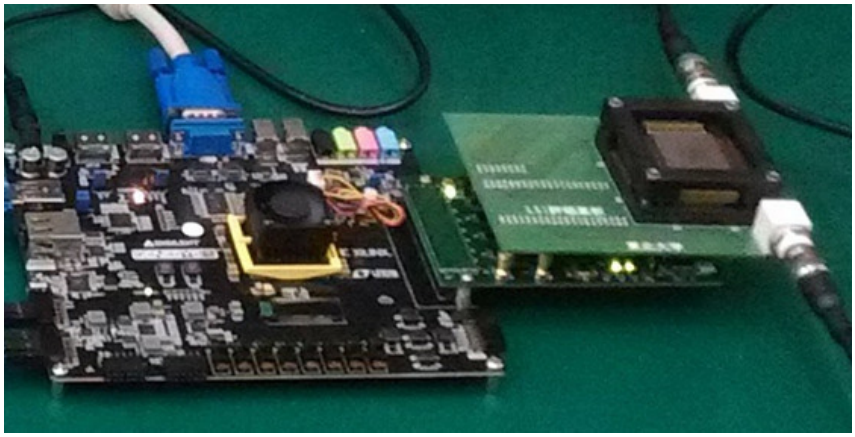

Fig. 14. Test environment using Digilent Genesys 2 FPGA and Keysight N6705B.

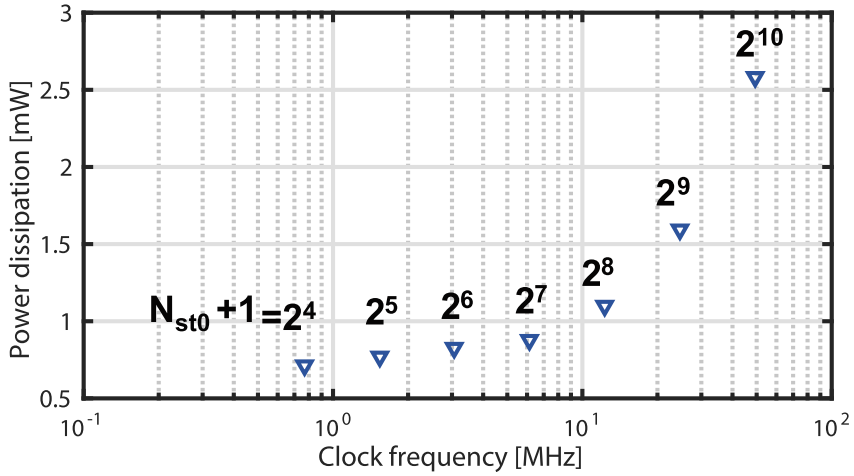

Fig. 15. Power dissipation vs. N_{sto} of the proposed chip with the supply voltage of 0.55V.

Figure 17 shows measured magnitude responses of the filterbank at channel 28 with N_{sto}=$2^{10}-1$, showing the symmetric feature of the gammatone filter and the asymmetric feature of the gammachirp filter. Figure 18 shows comparisons of magnitude responses of the filterbank at channel 28 between floating-point result and proposed stochastic result with N_{sto}=$2^{10}-1$. Figure 19 shows gain-compression features controlled by N_{sto} at channel 28. By changing N_{sto}, the gain compressions

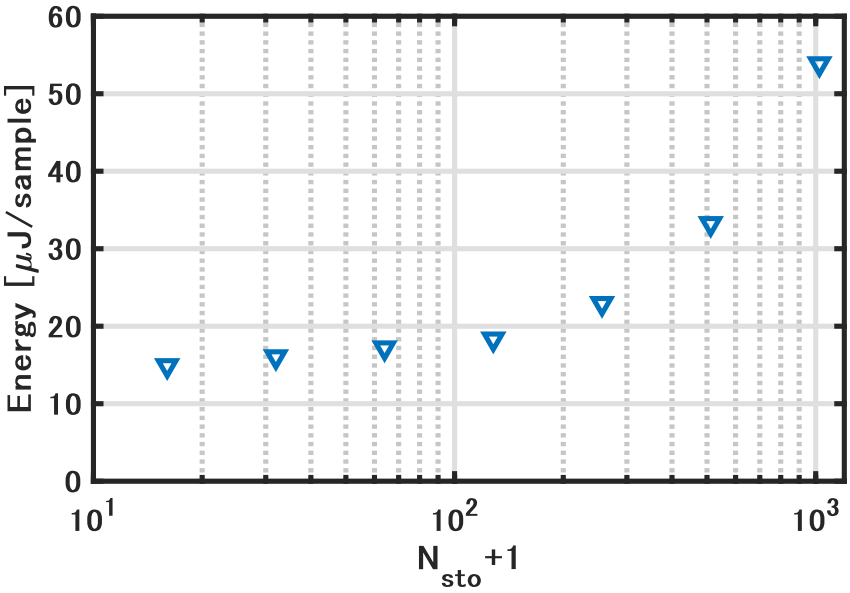

Fig. 16. Energy/sample vs. N_{sto} of the proposed chip with the supply voltage of 0.55V.

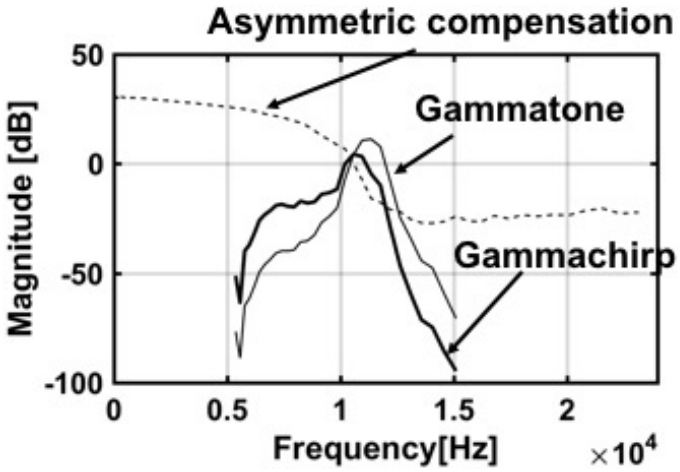

Fig. 17. Magnitude responses of the filterbank at channel 28 with N_{sto}=$2^{10}-1$.

are realized because smaller N_{sto} lowers the computation accuracy and hence the dynamic range.

Table I shows performance comparison tables with the related works [19–21]. All the conventional filterbanks are designed using analog circuits with different processes and configurations. In terms of the features, the proposed chip is the first silicon that realizes both asymmetric characteristic in frequency domain and gain compression depending on input acoustic pressures. Theoretically, the gammachirp filters can be designed using analog circuits. However, as the gammachirp filters are narrow-band bandpass filters, it is difficult to design high-performance gammachirp filters using analog circuits. It is because the narrow-band filters cause low dynamic ranges and high sensitivity in devices [32]. Using many analog devices, the filter characteristics could be improved, however, the circuit sizes would be unrealistic.

In terms of power dissipation per channel, the proposed circuit achieves around 6x smaller than the conventional work [19] that contains the gain compression feature. The area per channel of the proposed circuit is the 2nd smallest among the conventional works. In terms of technology scaling, it is hard for analog circuits to be scaled down because of the process variability. In contrast, the proposed stochastic filter can be further scaled down to recent technology nodes. The number of channels of the proposed filter is smaller than that of the conventional works due to the limitation of the size of the chip, however, it can be increased using larger chips. As a result, the proposed

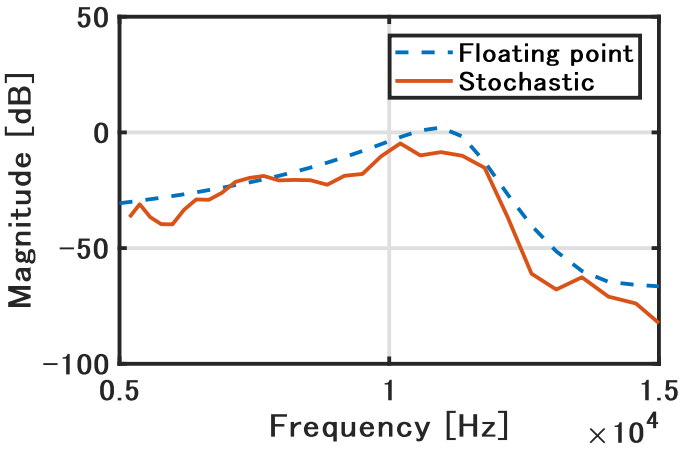

Fig. 18. Comparisons of magnitude responses of the filterbank at channel 28 between floating-point result and proposed stochastic result with N_{sto}=$2^{10}-1$.

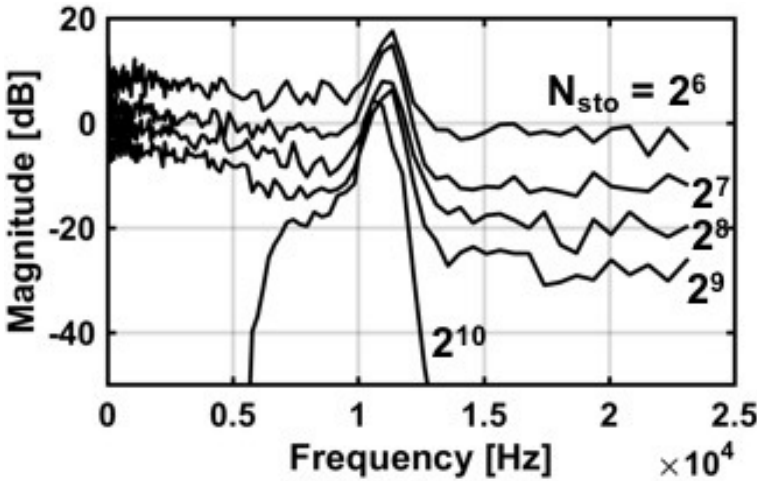

Fig. 19. Gain compression controlled by N_{sto} at channel 28.

Table I. Performance comparisons of auditory filterbanks.

	ISSCC' 06 [19]	TBCAS [20]	ISSCC' 16 [21]	This work
Circuit	Analog	Analog	Analog	Stochastic (digital)
Technology	0.25 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	65 nm CMOS
Power supply [V]	2.5	3.3	0.5	0.55
Channel number	360	64x2	64x2	32
Frequency range [Hz]	210-14k	50-50k	8-20k	20-20k
Power [μW]	52,000	12,000-22,000	595	715-2,585
Power per channel [μW]	144	94-172	4.4	22-81
Area [mm^2]	10.9	13.7	50.4	3.2
Area per channel [mm^2]	0.03	0.11	0.39	0.1
Power-area product per channel [μW*mm^2]	1560	1320-2420	232.1	71.5-258.5
Asymmetric characteristic	No	No	No	Yes
Gain compression depending	Yes	No	No	Yes

chip realizes both asymmetric characteristic in frequency domain and gain compression depending on input acoustic pressures while achieving the best power-area product per channel.

5. Conclusion

In this paper, the compressive gammachirp filterbank chip based on stochastic computation has been presented for brain-inspired area/power-efficient auditory signal processing. The FRNG technique reduces the noise signals at the output of the stochastic gammachirp filters by mitigating the randomness of stochastic computation, leading to the high gains with the short length of the stochastic bit streams. In addition, gain-compression characteristics depending on input acoustic pressures known as human auditory effects are naturally realized by changing the lengths of the stochastic bit streams. The proposed filterbank chip is fabricated using TSMC 65 nm CMOS process that achieves 715-2,585 μW with the sampling frequency of 48 kHz and the chip area of 3.2 mm^2. In comparison with the related works, the proposed chip is the first silicon that realizes both asymmetric characteristic in frequency domain and gain compression depending on input acoustic pressures while achieving the best power-area product per channel.

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